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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,327	09/28/2001	Alaa F. Alani	A2-4059 1496.00150	3179

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EXAMINER	
DAMIANO, ANNE L	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 03/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/966,327	ALANI ET AL.	
	Examiner	Art Unit	
	Anne L Damiano	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 12/20/04. These drawings are acceptable.

Note, figures 1 and 2 are clearly described in "Background of the Invention" section of the specification. Both figures are described as being "conventional" (Specification page 4: lines 1 and 19). Therefore, examiner does not see how Applicants' representative "does not necessarily agree" with the requirement to label FIGS 1 and 2 as "conventional."

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Schenck (6,072,329).

As in claim 1, Schenck discloses an apparatus comprising:

A circuit configured to (i) monitor a plurality of signals for transitions and (ii) invert said signals (transmit in complementary state) only when at least a predetermined number of said signals (The data lines are only transmitted in complementary state when more than half of the

data lines need to be switched from high to low or low to high.) transition in a predetermined direction (column 2: lines 16-30); and

A plurality of buffers configured to present said signals on a transmission bus (column 2: lines 28-30).

As in claim 2, Schenck discloses the apparatus according to claim 1, wherein said predetermined direction is one of (i) a high to low direction and (ii) a low to high direction (column 2: lines 20-23).

As in claim 3, Schenck discloses the apparatus according to claim 1, wherein said predetermined number is greater than one half of a total number of said signals (column 2: lines 22-24).

As in claim 4, Schenck discloses the apparatus according to claim 1, wherein said circuit comprises:

A transition checker circuit (comparison XOR gate) configured to present a plurality of transition signals each indicating a transition direction of one of said signals (column 5: lines 16-25);

A control circuit configured to present a flag signal (parity signals) when at least said predetermined number of said transition signals have said predetermined direction; and

An inverter circuit (adjustment XOR gate) configured to invert said signals in response to said flag signal (column 4: lines 1-23). (When the parity signal is a 1, data bits will be transmitted in the opposite direction from which it was received. Therefore, the parity signals are acting as flags that cause signals to be inverted.)

As in claim 5, Schenck discloses the apparatus according to claim 4, wherein said buffers are further configured to present said flag signal on said transmission bus (column 4: lines 45-53).

As in claim 6, Schenck discloses the apparatus according to claim 4, wherein said transition checker circuit comprises:

A plurality of flip-flops configured to present said signals as a plurality of sampled signals (column 4: lines 2-4);

A plurality of inverters (adjustment XOR) configured to present said signals as a plurality of inverted signals (column 6: lines 7-11); and

A plurality of logic gates configured to present said transition signals in response to said sampled signals and said inverted signals (column 4: lines 1-6).

As in claim 7, Schenck discloses the apparatus according to claim 4, wherein said circuit further comprises a plurality of flip-flops configured to store said signals as presented by said inverter circuit (column 4: lines 33-37).

As in claim 8, Schenck discloses the apparatus according to claim 7, wherein said circuit further comprises a clock configured to present a clock signal to said flip-flops (column 4: lines 33-37).

As in claim 9, Schenck discloses the apparatus according to claim 8, wherein said buffers are further configured to present said flag signal on said transmission bus and said transition checker circuit comprises:

A plurality of flip-flops configured to present said signals as a plurality of sampled signals (column 4: lines 2-4);

A plurality of inverters (adjustment XOR) configured to present said signals as a plurality of inverted signals (column 6: lines 7-11); and

A plurality of logical gates configured to present said transition signals in response to said sampled signals and said inverted signals (column 4: lines 1-23).

As in claim 10, Schenck discloses a method of reducing noise induced by transitions of a plurality of signals, the method comprising the steps of:

(A) monitoring said signals for said transitions;

(B) inverting said signals only in response (The data lines are only transmitted in complementary state when more than half of the data lines need to be switched from high to low or low to high.) to at least a predetermined number (more than half of the data lines) of said signals transitioning in a predetermined direction (column 2: lines 16-30); and

(C) presenting said signals on a transmission bus (column 2: lines 28-30).

As in claim 11, Schenck discloses the method according to claim 10, wherein said predetermined direction is one of (i) a high to low direction and (ii) a low to high direction (column 2: lines 20-22).

As in claim 12, Schenck discloses the method according to claim 10, wherein said predetermined number is greater than one half of a total number of said signals (column 2: lines 22-24).

As in claim 13, Schenck discloses the method according to claim 10, wherein step (A) comprises the sub-steps of:

Generating a plurality of transition signals each indicating a transition direction of one of said signals (column 5: lines 16-25); and

Generating a flag signal (parity signals) when at least said predetermined number of said transition signals have said predetermined direction (column 4: lines 7-23). (When the parity signal is a 1, data bits will be transmitted in the opposite direction from which it was received. Therefore, the parity signals are acting as flags that cause signals to be inverted.)

As in claim 14, Schenck discloses the method according to claim 13, further comprising the step of presenting said flag signal on said transmission bus (column 4: lines 45-53).

As in claim 15, Schenck discloses the method according to claim 13, wherein presenting said plurality of transition signals comprises the sub-steps of:

Sampling said signals to present a plurality of sampled signals (column 4: lines 2-4);

Inverting said signals to present a plurality of inverted signals (column 6: lines 7-11); and

Logically combining said sampled signals and said inverted signals to present said transition signals (column 4: lines 1-6).

As in claim 16, Schenck discloses the method according to claim 13, further comprising the step of storing said signals prior to presenting said signal on said transmission bus (column 4: lines 33-37).

As in claim 17, Schenck discloses the method according to claim 16, further comprising the step of generating a clock signal to control said storing (column 4: lines 33-37).

As in claim 18, Schenck discloses an integrated circuit comprising:

Means for monitoring a plurality of signals for transitions;

Means for inverting said signals only (The data lines are only transmitted in complementary state when more than half of the data lines need to be switched from high to low or low to high.) in response to at least a predetermined number of said signals transitioning in a predetermined direction (column 2; lines 16-30); and

Means for presenting said signals on a transmission bus (column 4: lines 1-23).

As in claim 19, Schenck discloses the integrated circuit according to claim 18, wherein said predetermined direction is one of (i) a high to low direction and (ii) a low to high direction (column 2: lines 20-22).

As in claim 20, Schenck discloses the integrated circuit according to claim 18, wherein said means for monitoring comprising:

Means for presenting a plurality of transition signals each indicating a transition direction of one of said signals (column 4: lines 7-23). (When the parity signal is a 1, data bits will be transmitted in the opposite direction from which it was received. Therefore, the parity signals are acting as flags that cause signals to be inverted.)

Response to Arguments

4. Applicant's arguments filed 12/20/04 have been fully considered but they are not persuasive.

Regarding the first argument addressing claims 1, 10 and 18, the purpose of Schenck's system is to minimize switching noise by inverting data lines *only* when more than half of the lines are required to switch, thereby reducing switching noise without having to switch more than half of the data lines are any time (column 2: lines 16-30 and column 3: lines 3-6).

Applicant pointed to column 6: lines 44-61 to allege that Schenck is contemplating inverting bus signals. However, column 6: lines 44-61 is demonstrating how the voting system

works to invert the signals when more than half of the comparison signals vote to switch the parity signal. No where in Schenck is it disclosed that the signals will not be inverted if more than half are required to be switched from high to low or low to high.

Regarding the second argument, addressing claims 4 and 13, Schenck clearly describes a transition checker circuit in the comparison XOR gate. See claim rejection above.

Regarding the third argument addressing claims 6, 9 and 15, Schenck clearly describes flip-flops, inverted signals and logic gates responsive to the inverted signals and the sample signals. See claim rejection above.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anne L Damiano whose telephone number is (571) 272-3658. The examiner can normally be reached on M-F 9-6:30 first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ALD

SCOTT BADERMAN
PRIMARY EXAMINER